Logic Synthesis for Reconfigurable Transistors

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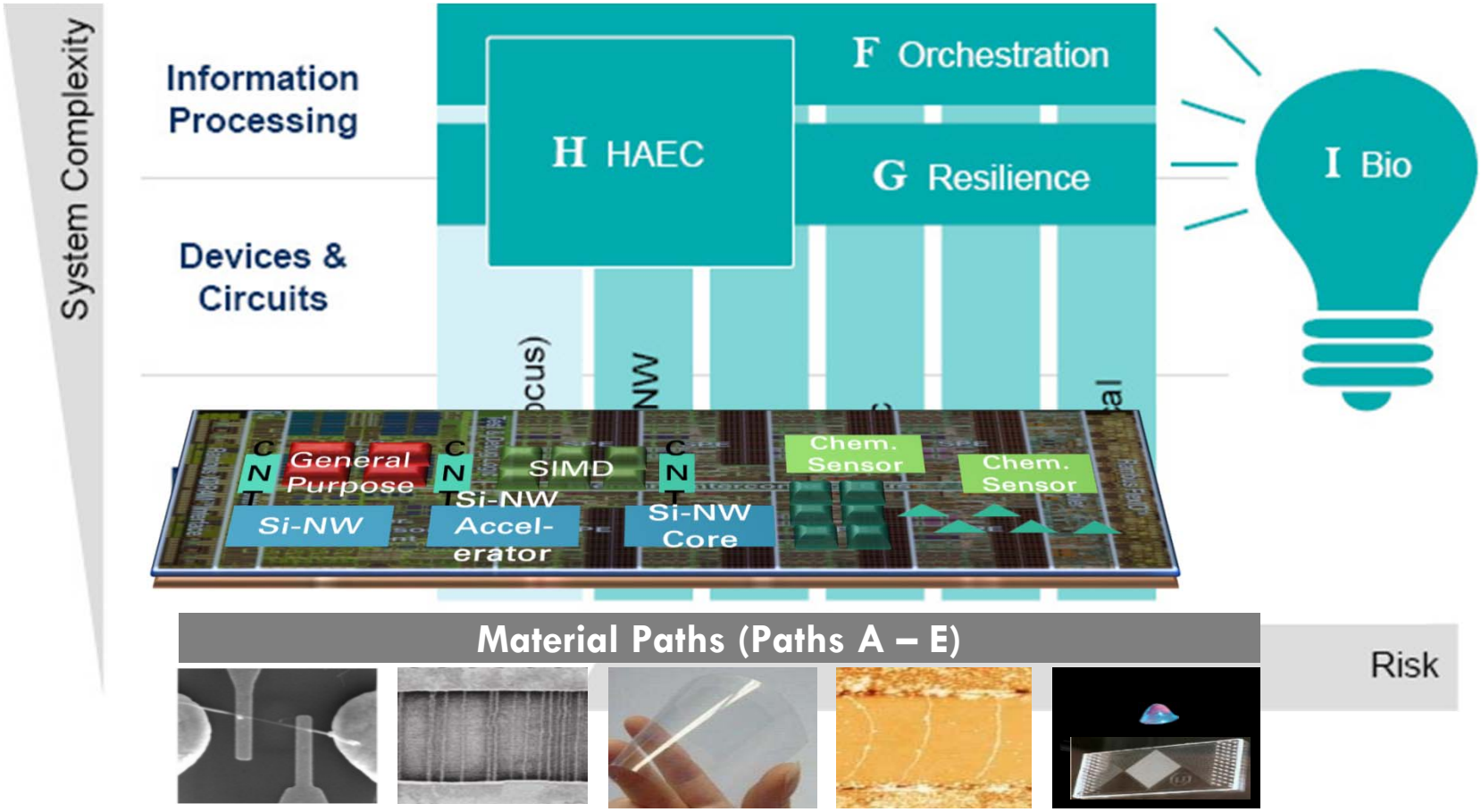
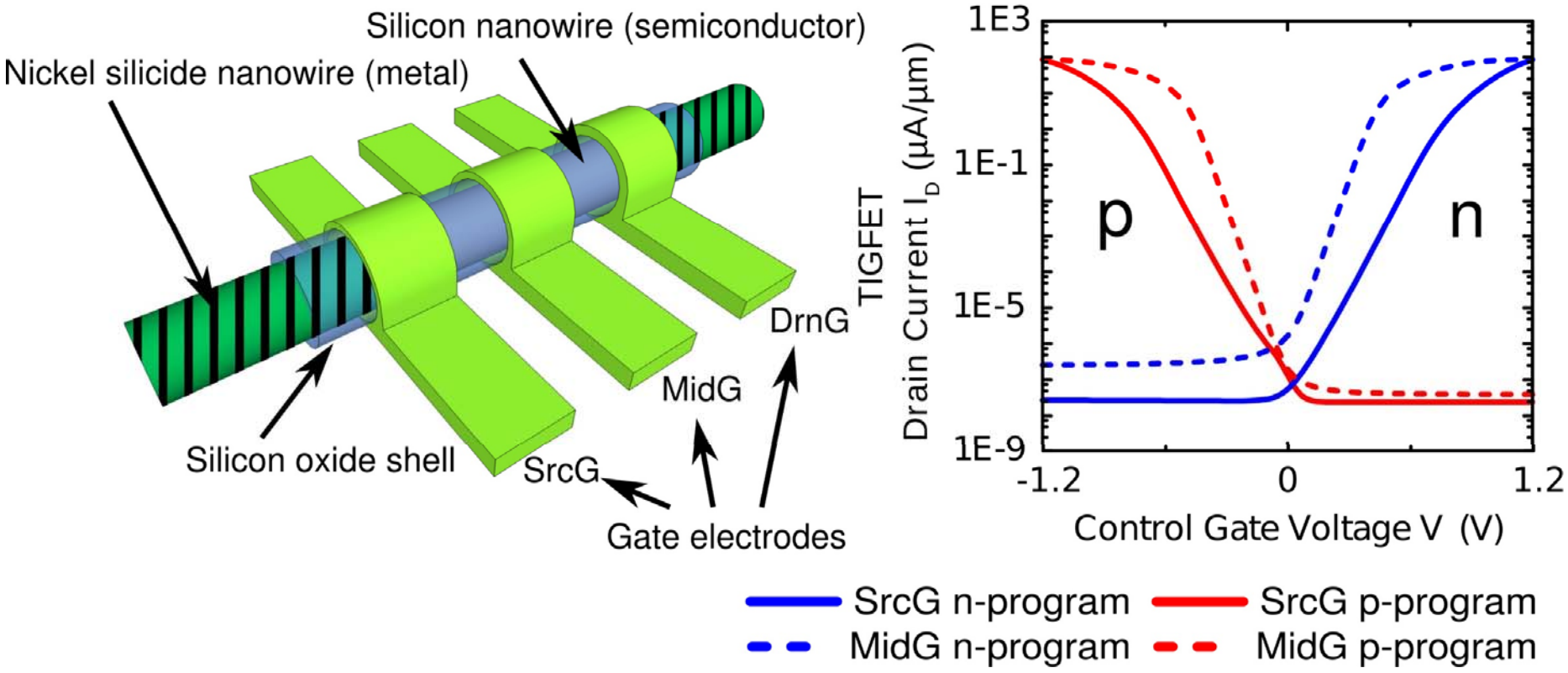
CFAED: Center for Advancing Electronics Dresden



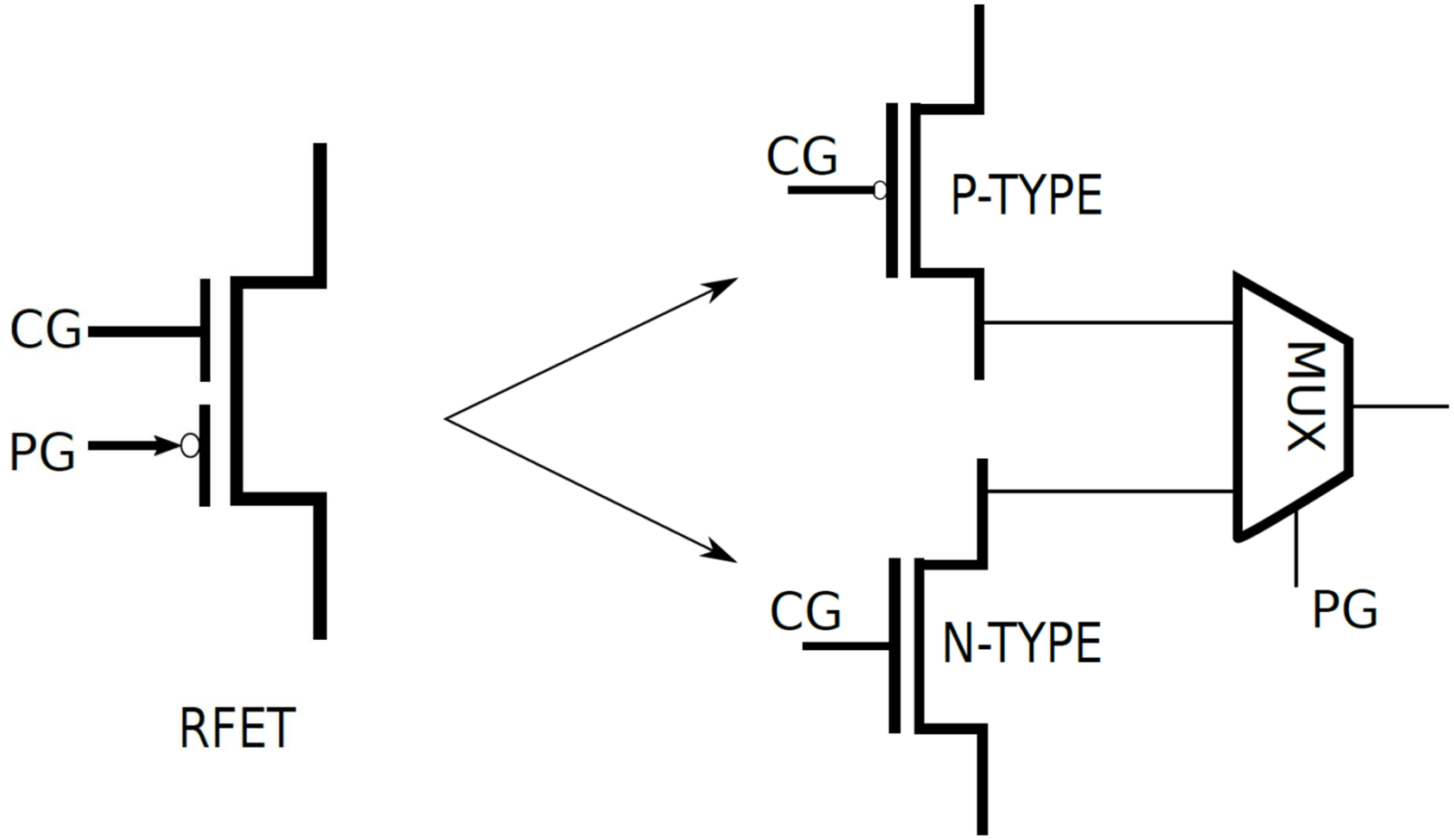
What will we learn today?

- Where does the reconfigurability come from?
- Designing novel combinational gates
- How does it benefit us?
- Going beyond logic synthesis
- Where are we going from here?

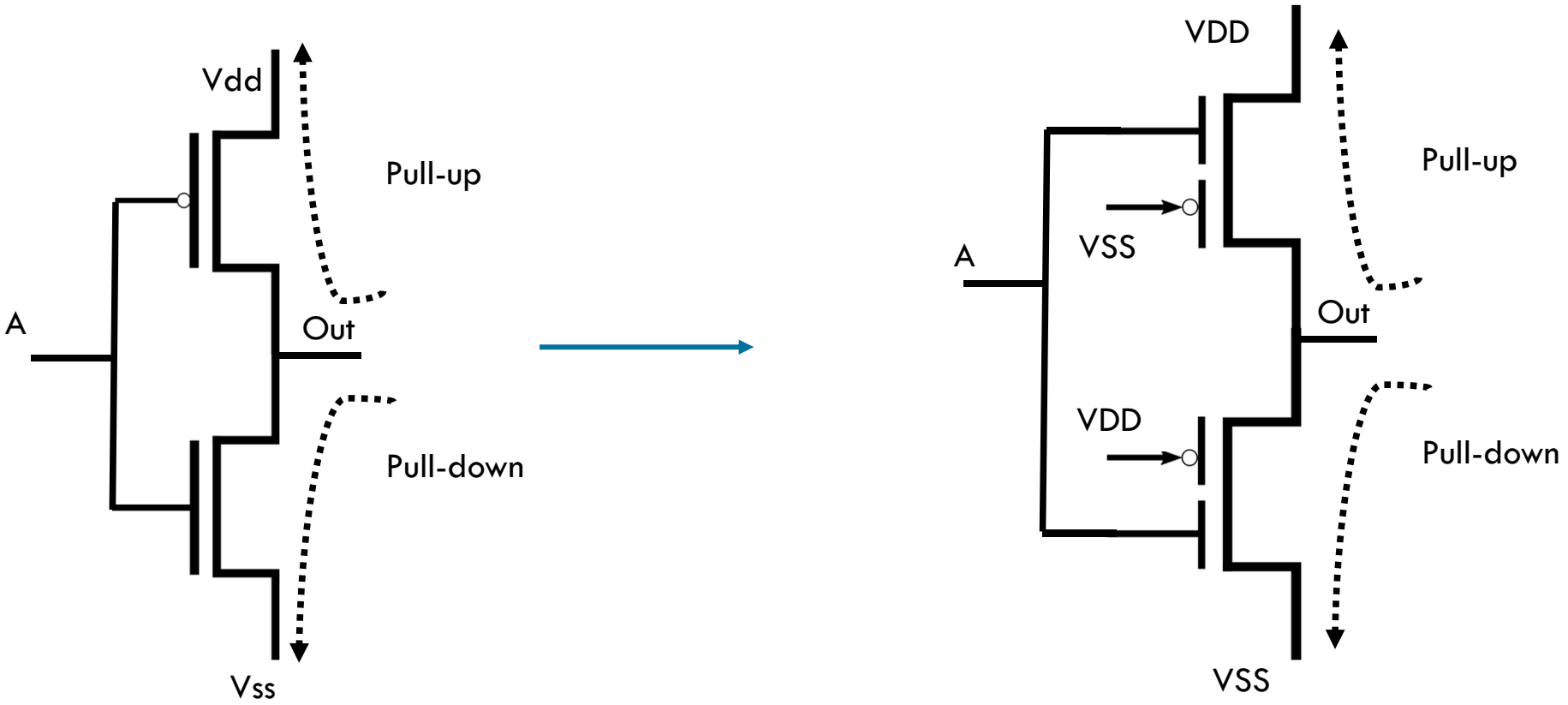
Reconfigurable Transistors: Silicon Nanowires Based Reconfigurable FETs



SiNW Dual-gate RFETs: Combines p-type and n-type functionality

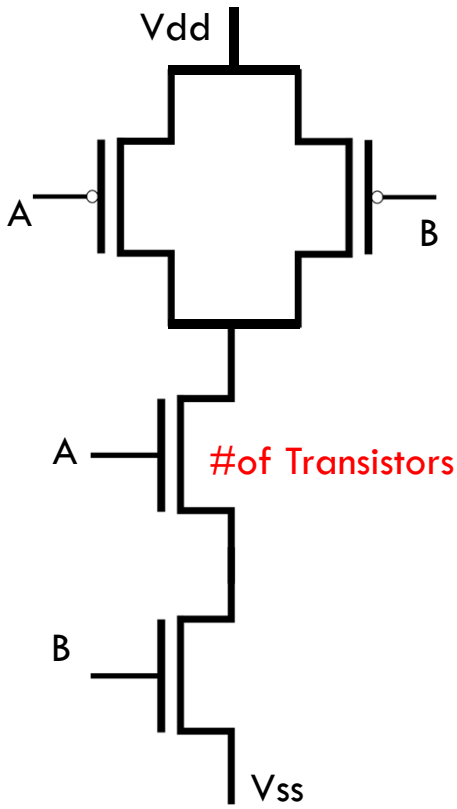


Dual-Gate RFETs based Inverter



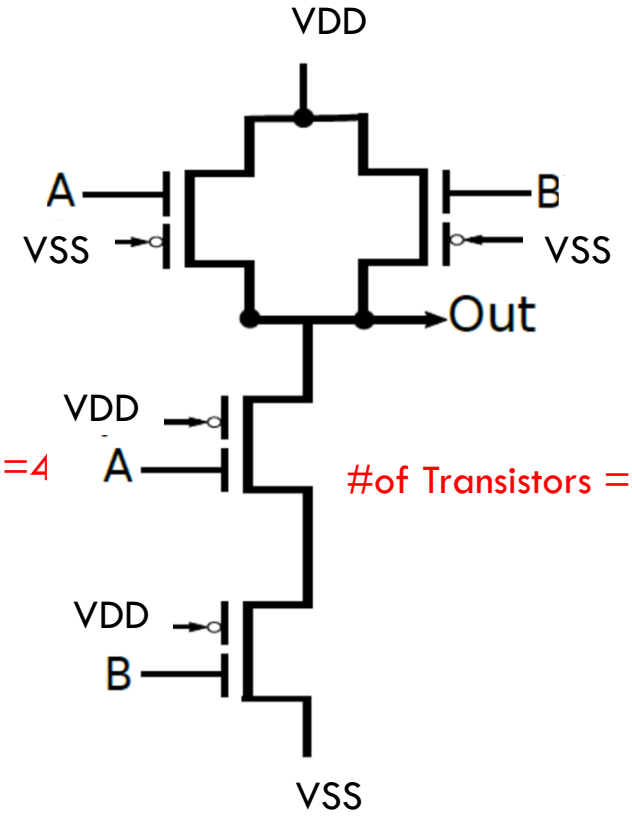
CMOS Based Inverter

Multi Input Gate RFETs: NAND



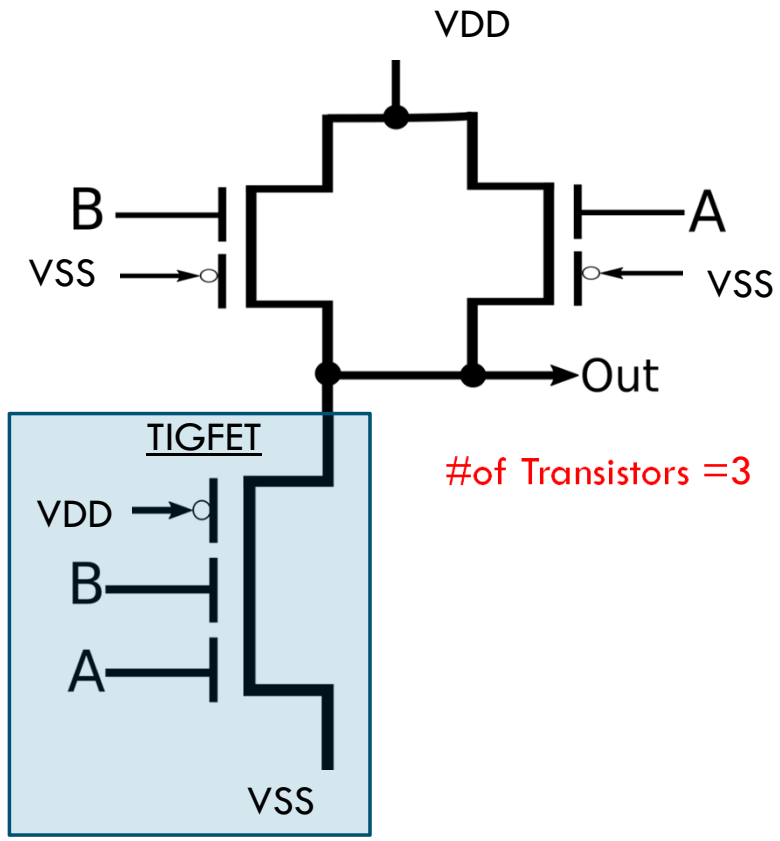
#of Transistors =4

CMOS



#of Transistors =4

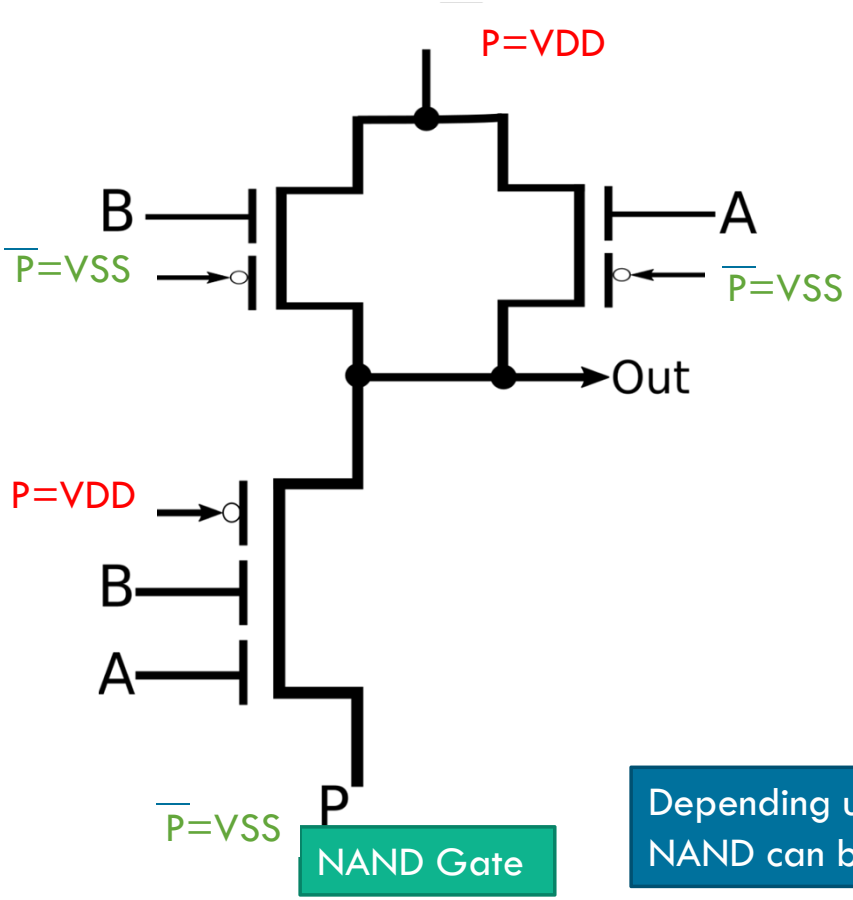
SiNW with Dual Gate RFET



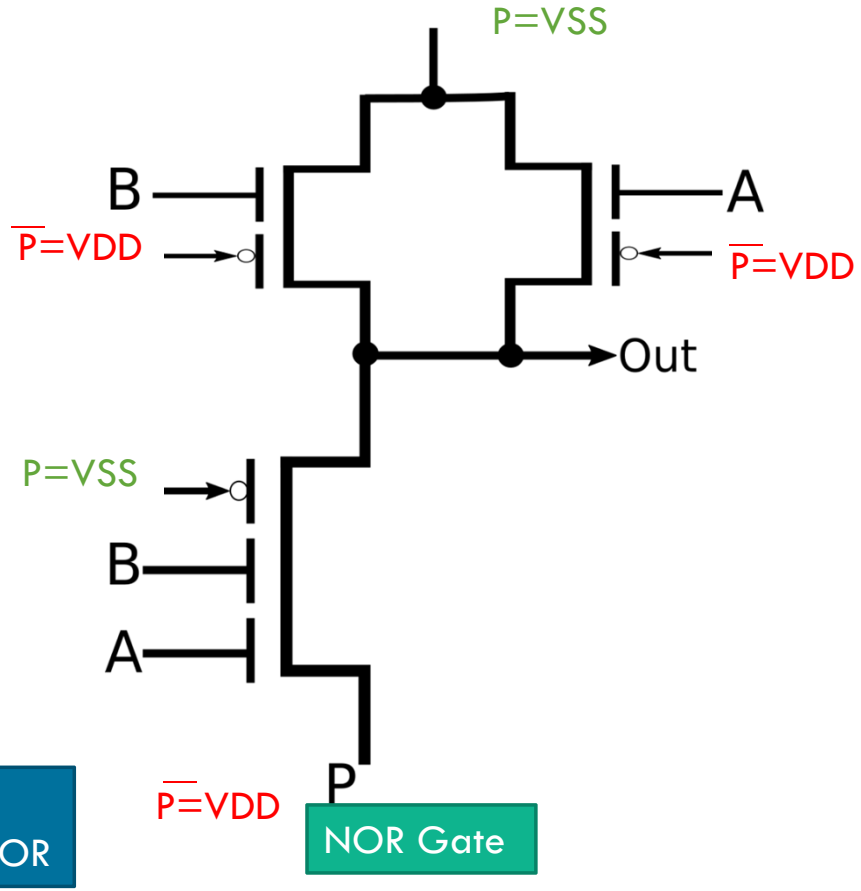
#of Transistors =3

SiNW with TIGFET

Reconfigurable Gate

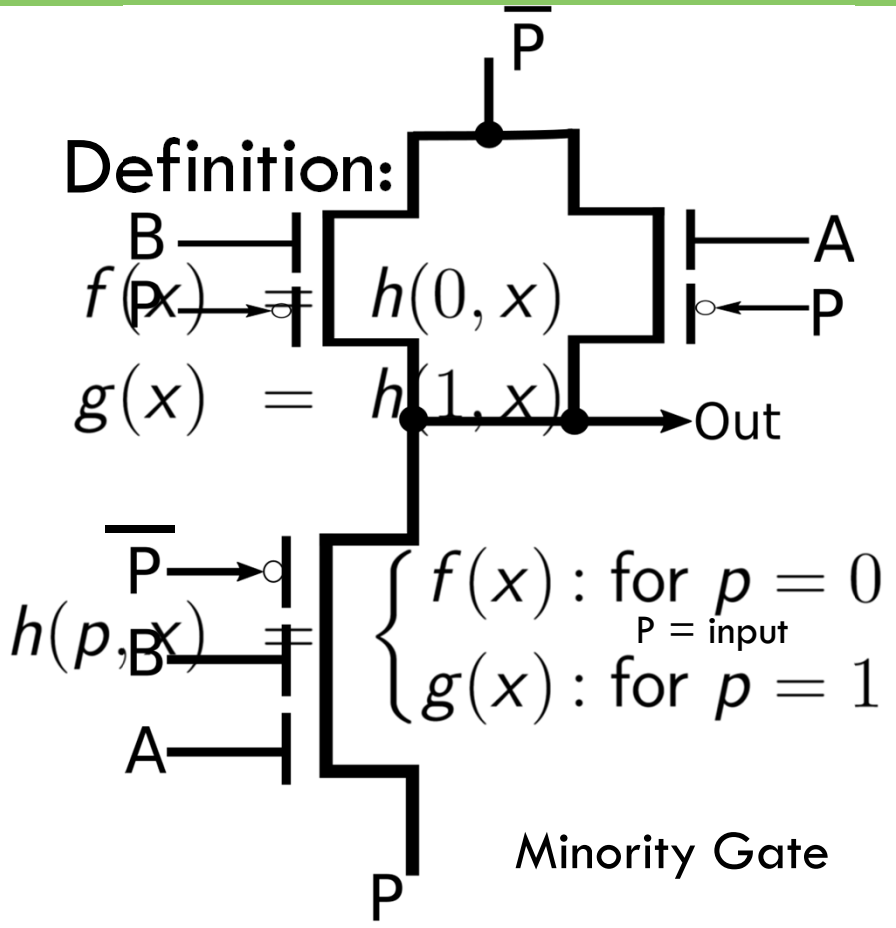


Depending upon value of P, NAND can be configured as NOR



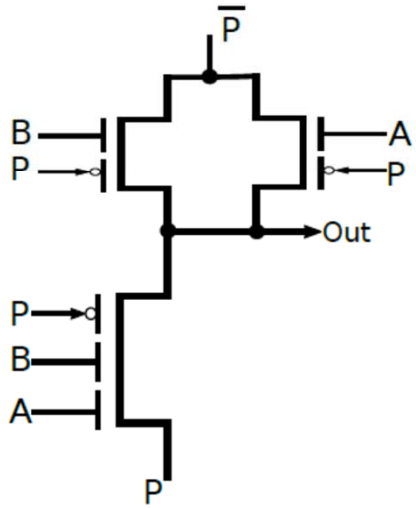
Reconfigurability: Mathematical Representation

	A	B	P	Out ≡ 3-MIN
NAND	0	0	0	1
	0	1	0	1
	1	0	0	1
	1	1	0	0
NOR	0	0	1	1
	0	1	1	0
	1	0	1	0
	1	1	1	0

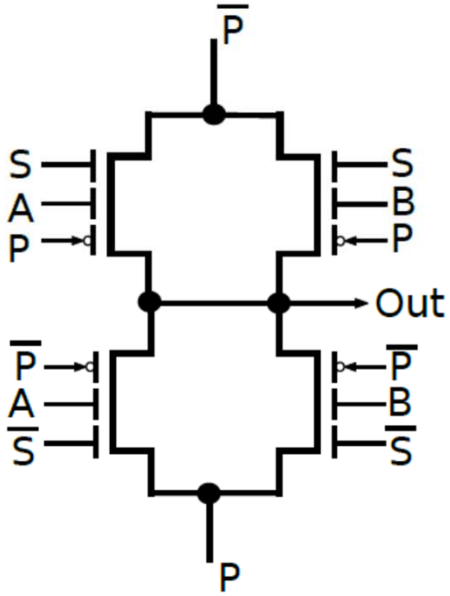


Other Combinational logic Gates

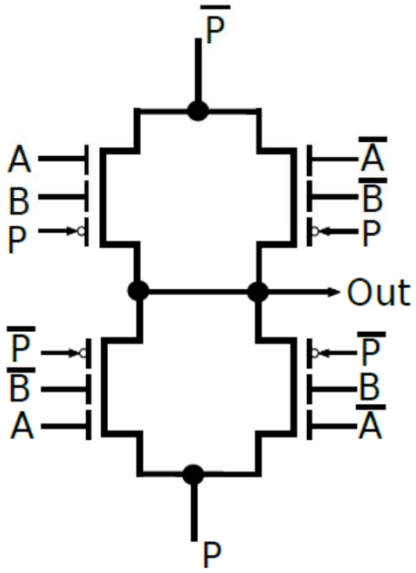
a) 2NAND(P=0)
2NOR(P=1)
3Min(P=input)[slow]



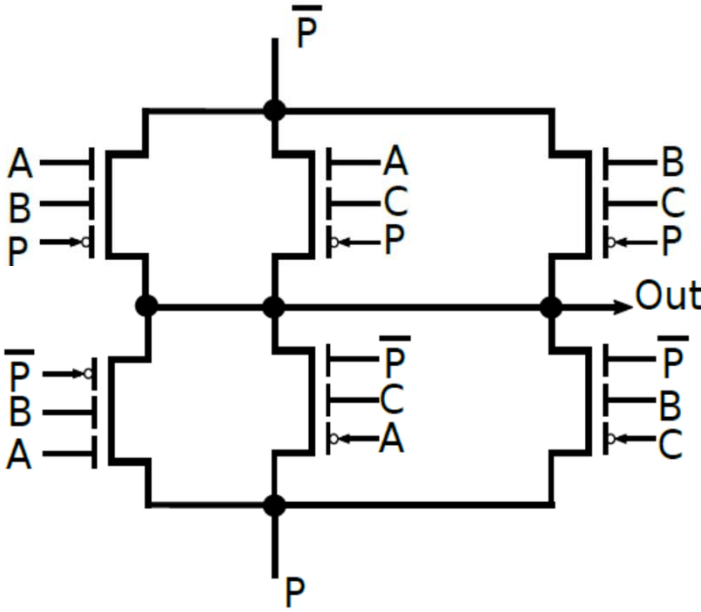
b) 2MUX (P =1)



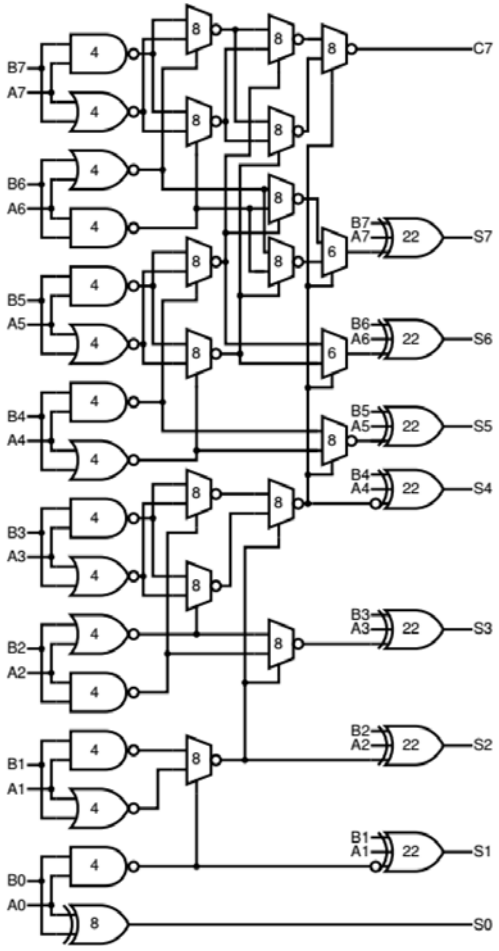
c) 2XOR(P = 1)
2XNOR(P = 0)
3XOR (P = Input)



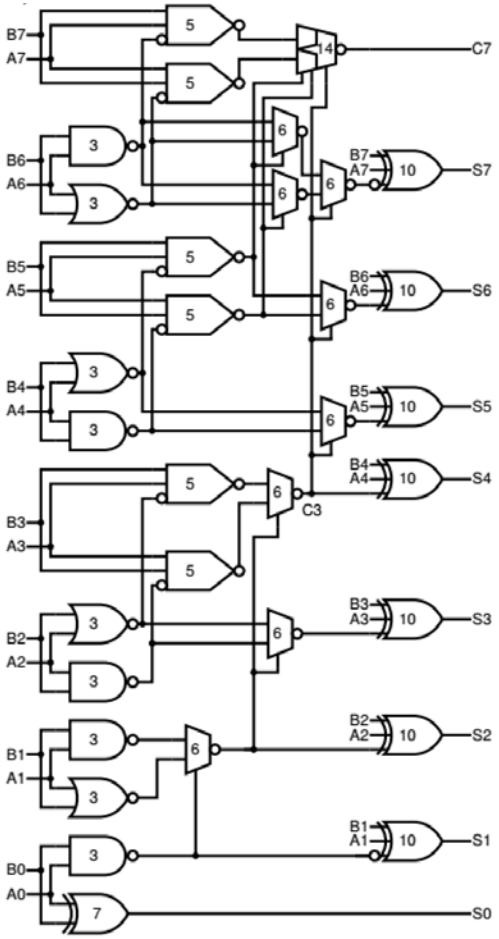
d)3MAJ(P =1)
3MIN(P=0)



Case Study: Conditional Carry Adder



#of Transistors
=352



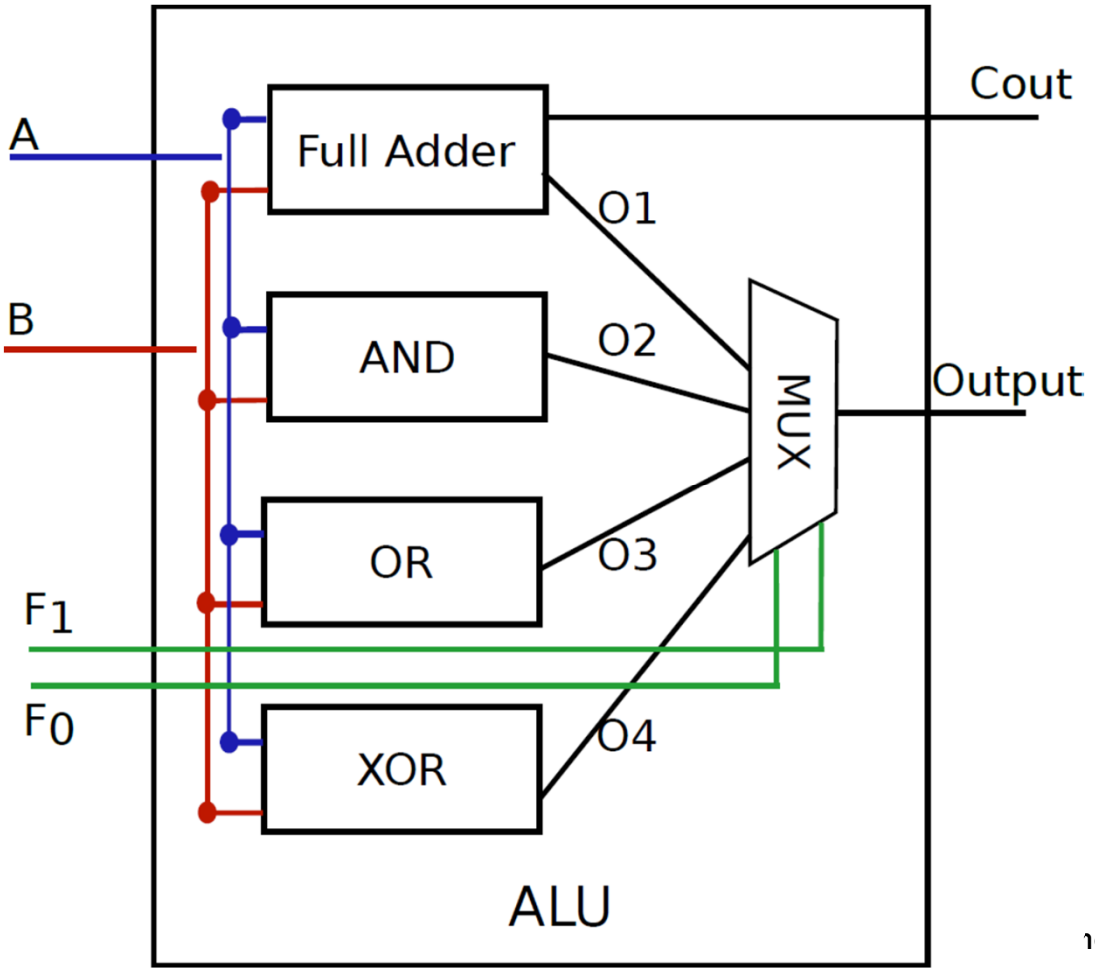
#of Transistors
=196

SiNW RFETs vs CMOS

*Using logical effort theory

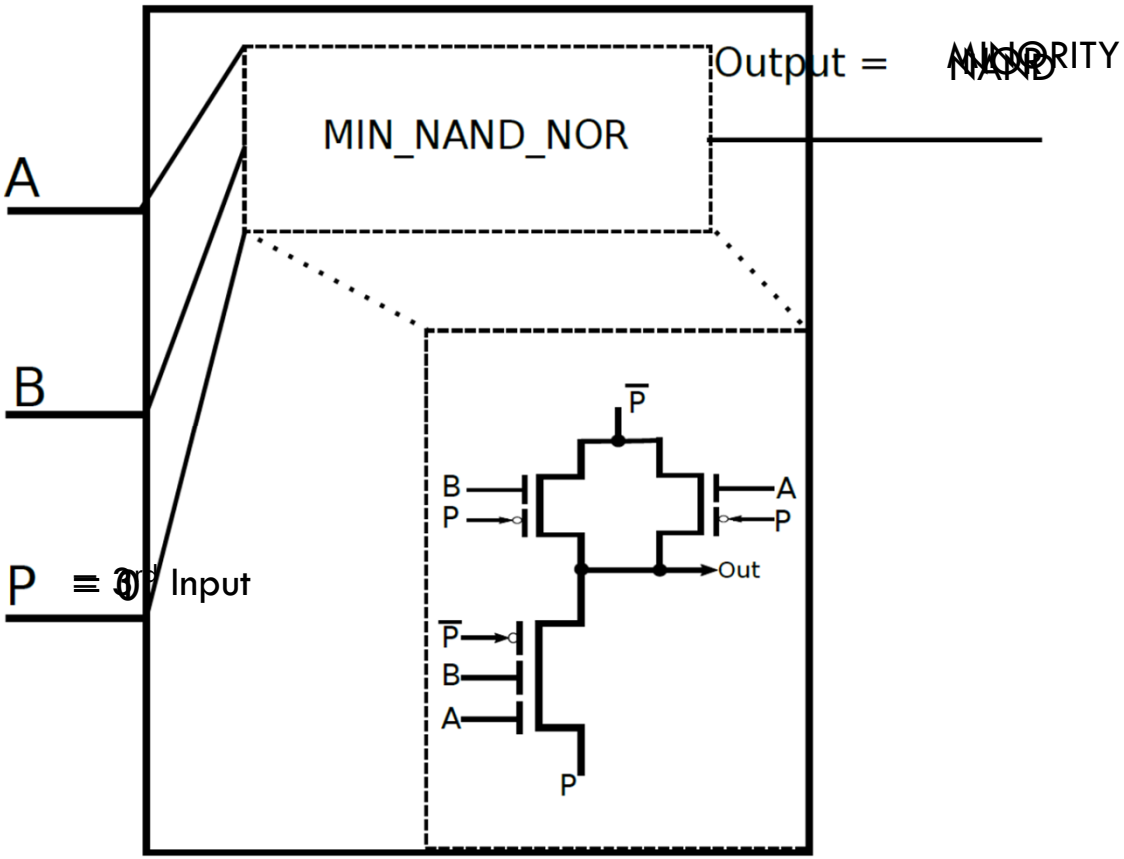
Extrinsic Reconfigurability

- Extrinsic Reconfigurability
  - Change some bits in the control path
  - Extra circuitry req. here

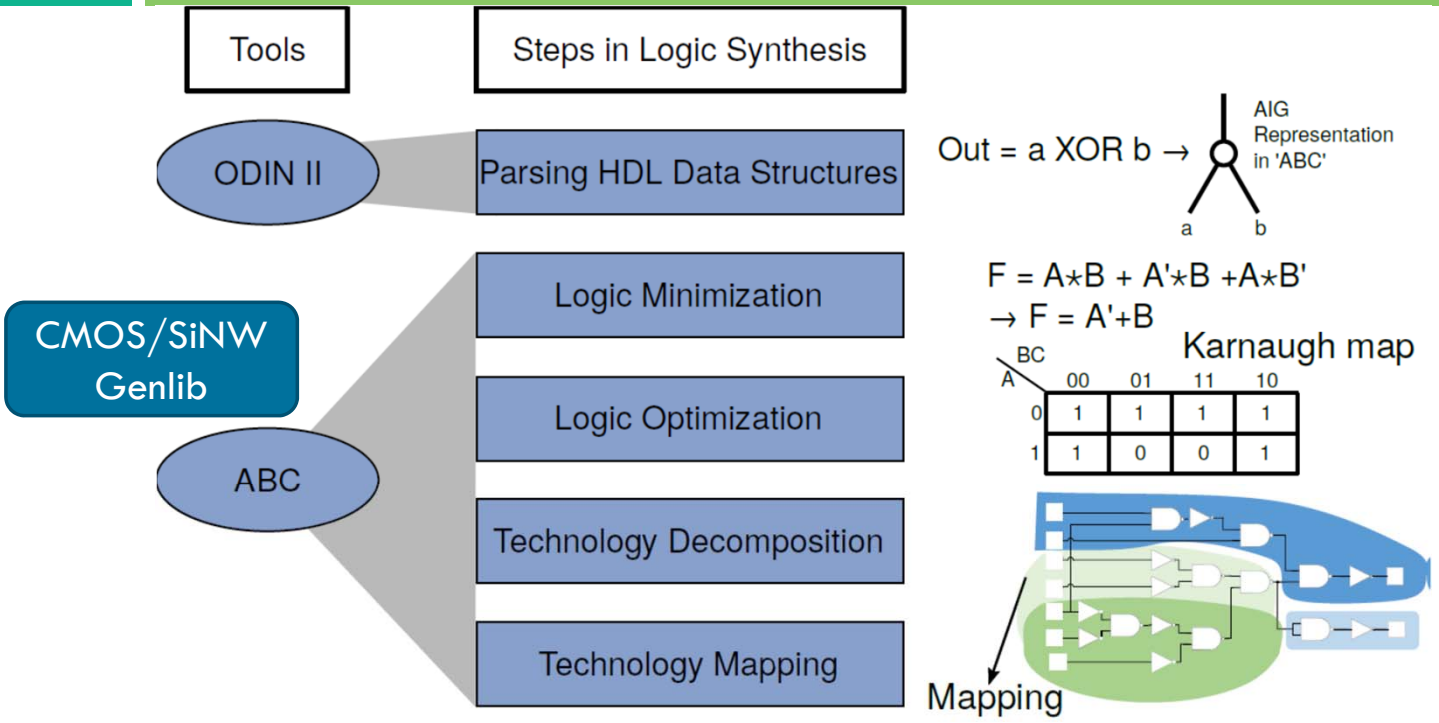


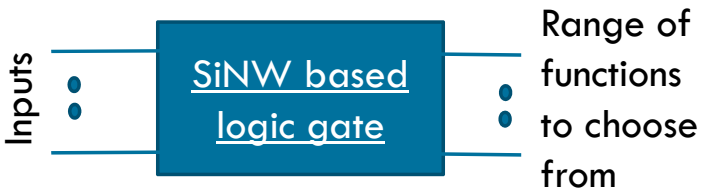
Intrinsic Reconfigurability

- Intrinsic reconfigurability
  - Unique electrical properties from the material
  - No extra circuitry.

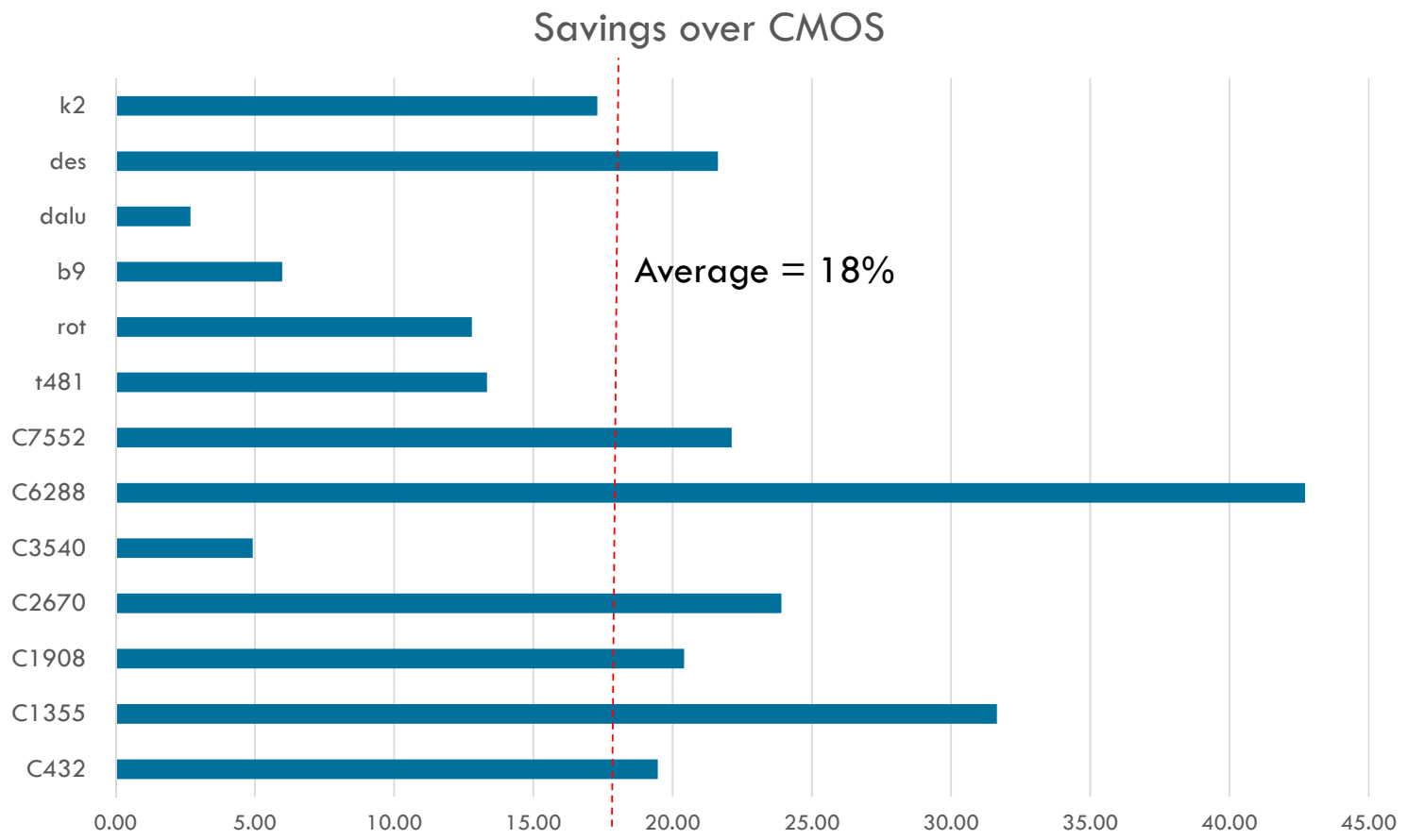


Design Flow

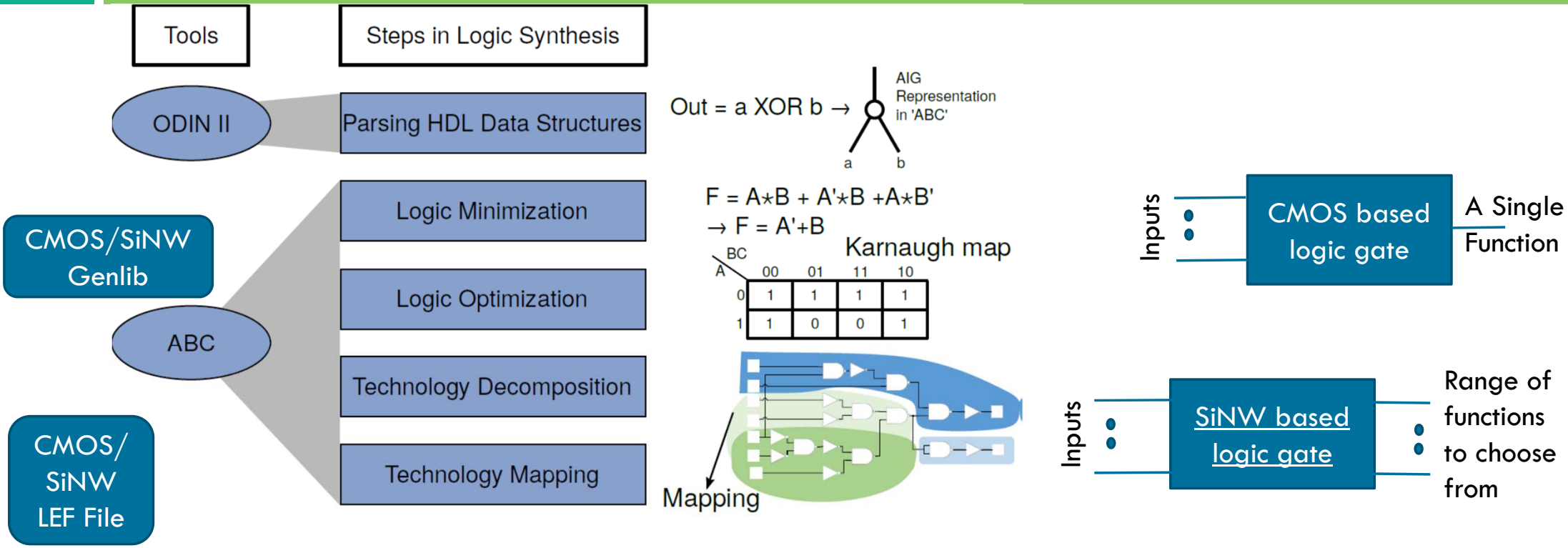




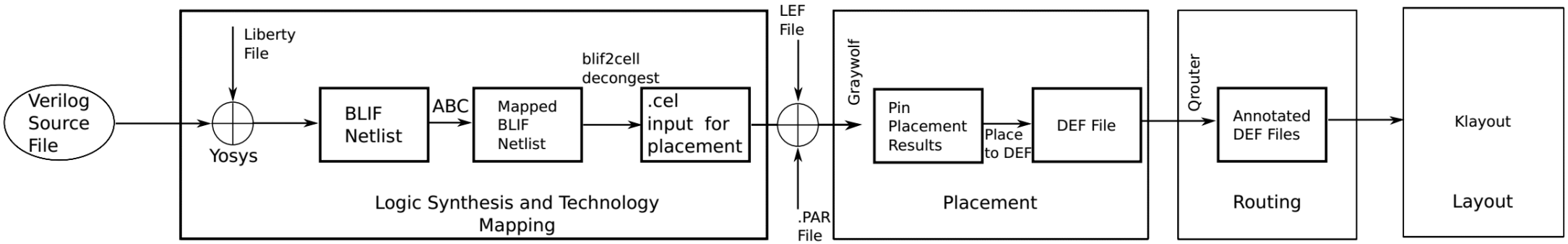
Area savings over CMOS – post logic synthesis



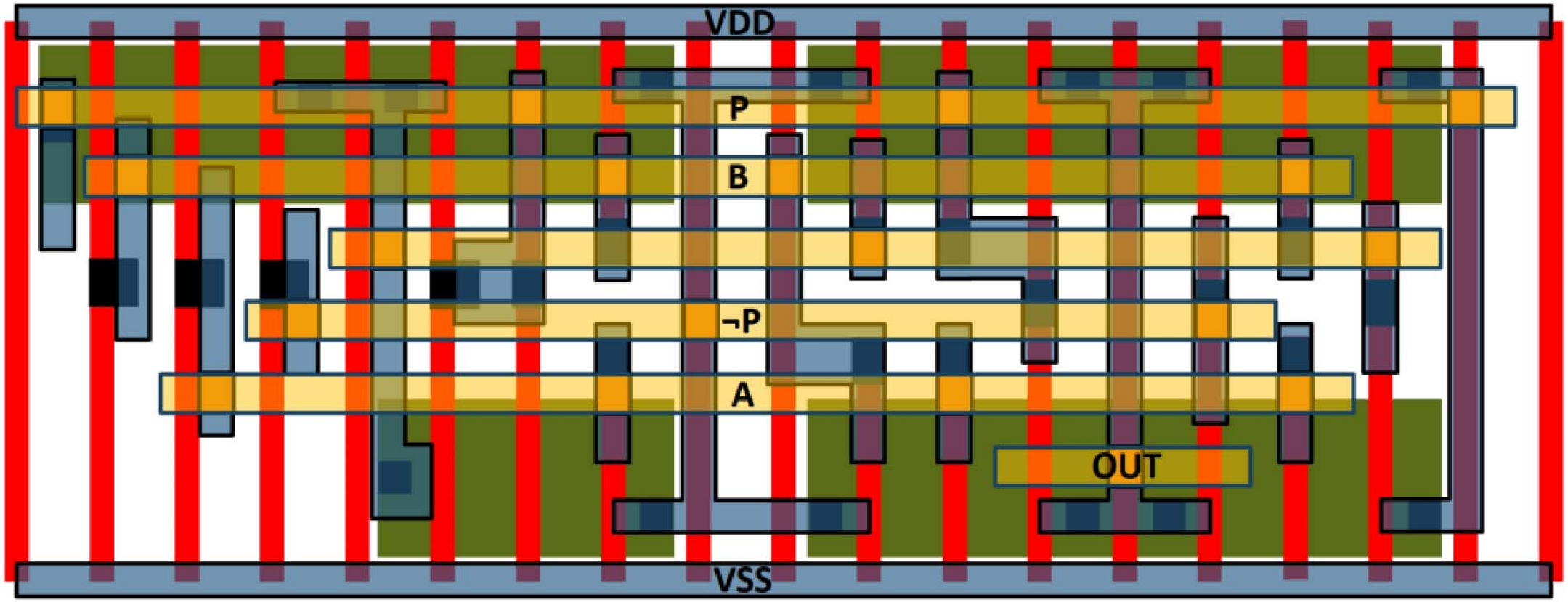
Design Flow: Adding place and route



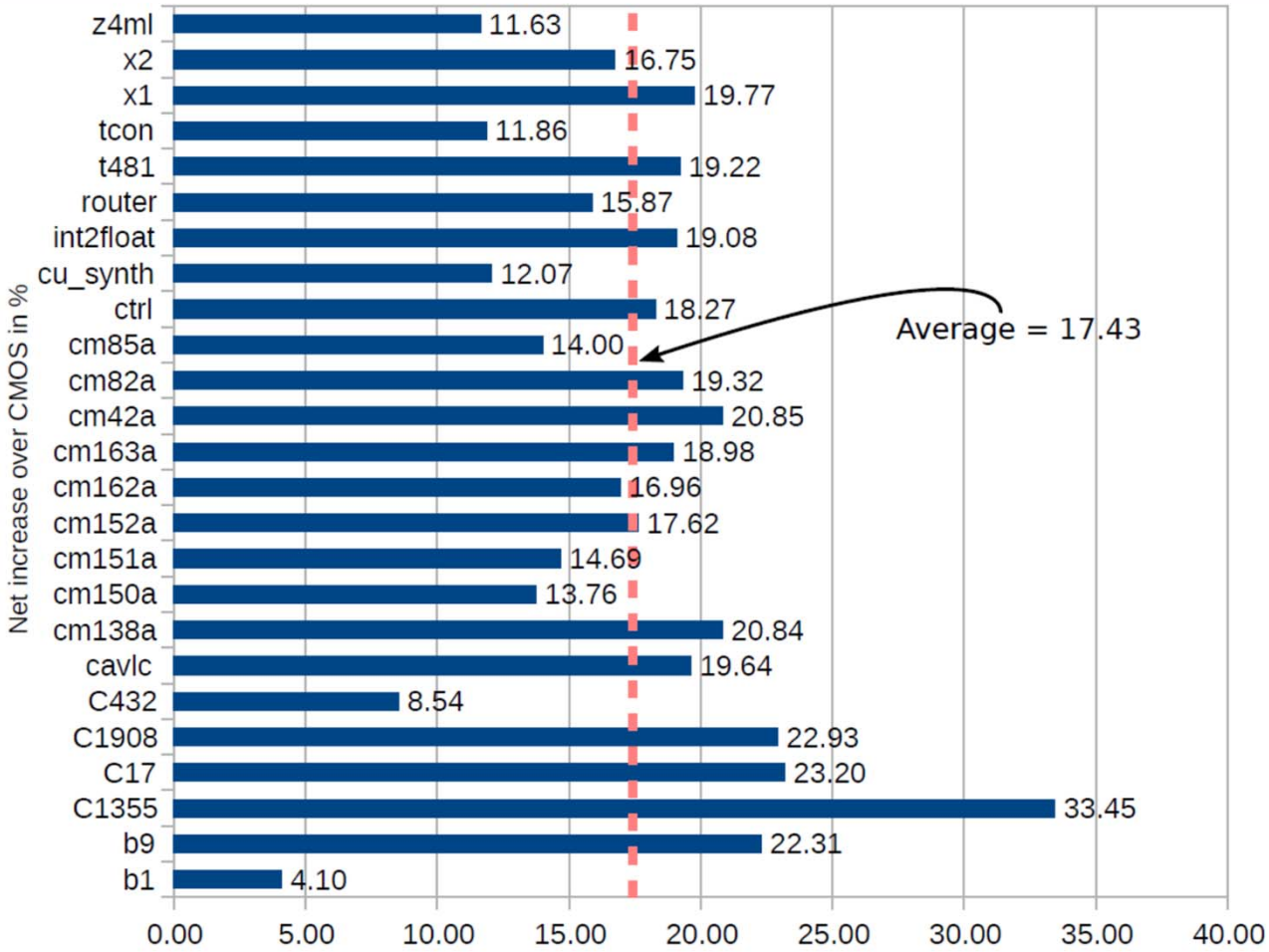
Physical Synthesis Flow



SiNW XOR Layout Concept



Area increase over CMOS – post P&R

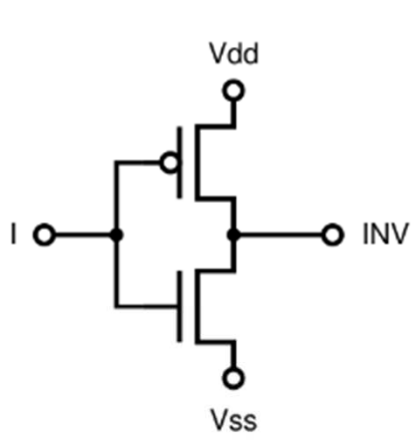


Other Ongoing Works – Property Checking

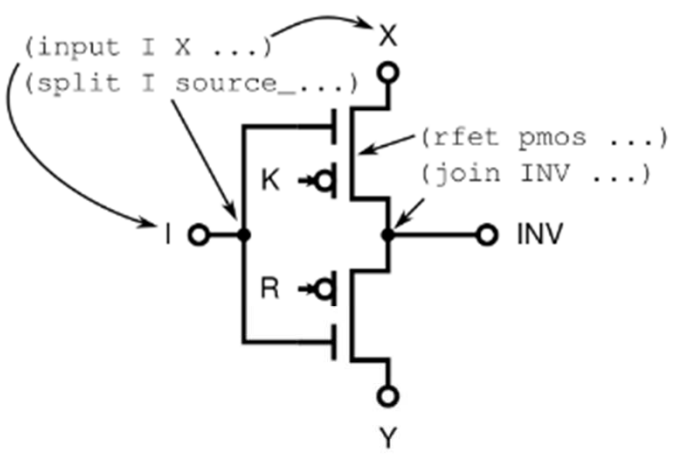
1. Exploring design space of new standard cells, exploiting reconfiguration
   a. By using meta-models that represent a multitude of possible circuit topologies
   b. Enumeration of all distinct Boolean formulae that can be implemented with a specific meta-model
2. Quantifying found cells using probabilistic transistor models
   a. Approach is agnostic to a specific technology
   b. New switching functions / characteristics can be easily added
   c. (Probabilistic) delay and activity are possible targets

Other Ongoing Works – Property Checking

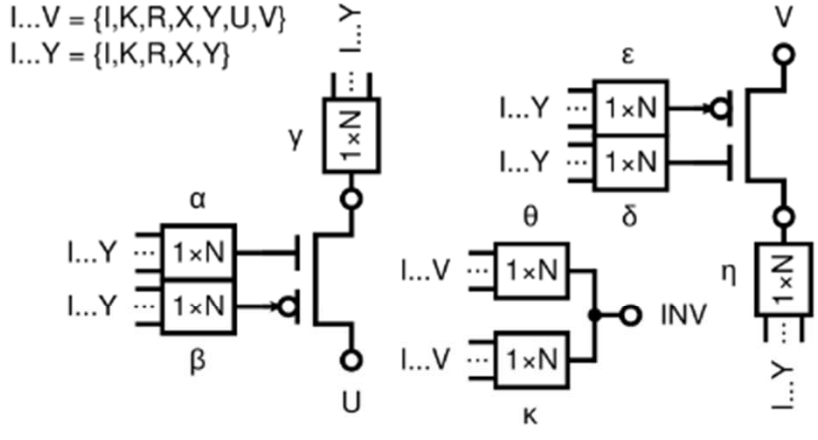
Q: Is it possible to implement an Inverter with each of these circuits?



A: Yes! (Obviously)
The input is the solution.

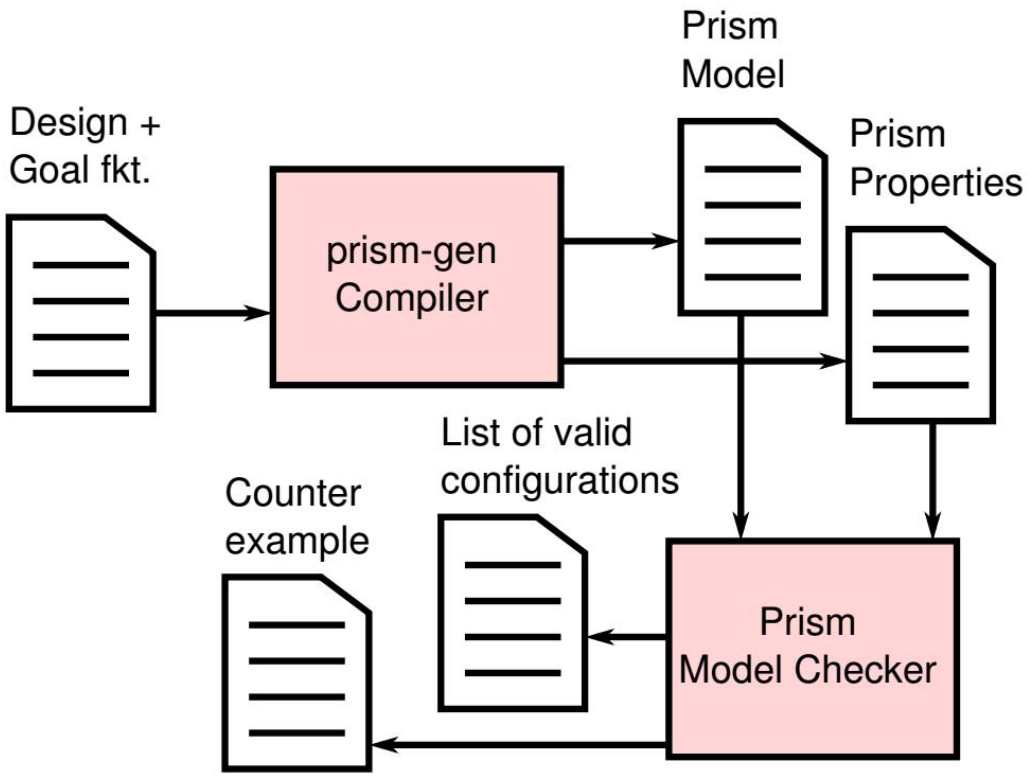


A: Yes!
Solutions = {(R,X=1;K,Y=0),
(R,X=0;K,Y=1)}



A: Yes!
Solutions = {(α = I; β = 1; γ = 0; δ = I; ε = 0; η = 1; θ = U; κ = V),
(α = I; β = 1; γ = 0; δ = I; ε = 0; η = 1; θ = V; κ = U),
(α = I; β = 0; γ = 1; δ = I; ε = 1; η = 0; θ = U; κ = V),
(α = I; β = 0; γ = 1; δ = I; ε = 1; η = 0; θ = V; κ = U)}

Other Ongoing Works – Property Checking



Other Ongoing Works – Security

- Use the program gate to camouflage circuits
- Only a particular key to activate the circuit
  - Length of the key can be used as a tunable knob
- Other keys may to be used to de-activate (kill-switch) the chip
- Camouflaging also makes it hard to reverse-engineer a circuit

Conclusions

- Important to re-visit logic synthesis for emerging technologies
- Exploit ambi-polarity of transistors to make smaller (faster?) circuits
- Need to consider post P&R results for a true evaluation
- Need better/realistic models of emerging devices

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Questions and Answers

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